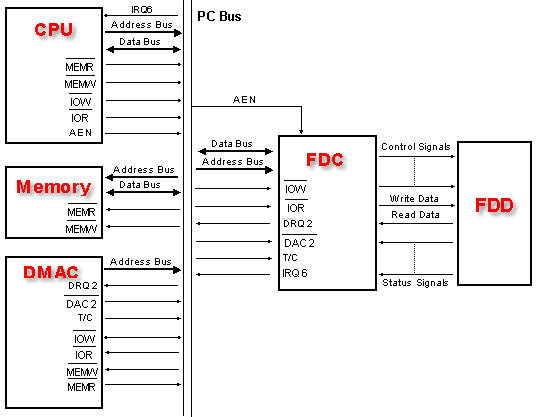
**Floppy disk interface**

[](https://en.wikipedia.org/wiki/File:Fdcinpc.jpg)A single floppy-disk controller (FDC) board can support up to four [floppy disk drives](https://en.wikipedia.org/wiki/Floppy_disk_drive). The controller is linked to the [system bus](https://en.wikipedia.org/wiki/System_bus) of the computer and appears as a set of [I/O](https://en.wikipedia.org/wiki/Input/output) ports to the [CPU](https://en.wikipedia.org/wiki/Central_processing_unit). It is often also connected to a channel of the [DMA](https://en.wikipedia.org/wiki/Direct_memory_access) controller. On the [x86](https://en.wikipedia.org/wiki/X86) PC the floppy controller uses [IRQ](https://en.wikipedia.org/wiki/Interrupt_request) 6, on other systems other [interrupt](https://en.wikipedia.org/wiki/Interrupt) schemes may be used. The floppy disk controller usually performs data transmission in [direct memory access](https://en.wikipedia.org/wiki/Direct_memory_access) (DMA) mode.

***Fig: Block diagram showing FDC communication with the CPU and the FDD.***

Most of the floppy disk controller (FDC) functions are performed by the [integrated circuit](https://en.wikipedia.org/wiki/Integrated_circuit) but some are performed by external hardware circuits. The list of functions performed by each is given below.

**Floppy disk controller functions (FDC)**

* Translate data bits into [FM](https://en.wikipedia.org/wiki/Digital_frequency_modulation), [MFM](https://en.wikipedia.org/wiki/Modified_Frequency_Modulation), [M²FM](https://en.wikipedia.org/wiki/Modified_Modified_Frequency_Modulation), or [GCR](https://en.wikipedia.org/wiki/Group_coded_recording) format to be able to record them
* Interpret and execute commands such as seek, read, write, format, etc.
* Error detection with [checksums](https://en.wikipedia.org/wiki/Checksums) generation and verification, like [CRC](https://en.wikipedia.org/wiki/Cyclic_redundancy_check)

**External hardware functions**

* Selection of [floppy disk drive](https://en.wikipedia.org/wiki/Floppy_disk_drive) (FDD).
* Switching-on the floppy drive motor.
* Reset signal for the floppy controller IC.
* Enable/disable interrupt and DMA signals in the floppy disk controller (FDC)
* Data separation logic
* [Write pre-compensation](https://en.wikipedia.org/wiki/Write_precompensation) logic
* [Line drivers](https://en.wikipedia.org/wiki/Line-level) for signals to the controller
* Line receivers for signals from the controller

Input/output ports for common x86-PC controller

The FDC has three [I/O](https://en.wikipedia.org/wiki/I/O) ports. These are:

* Data port
* Main status register (MSR)
* Digital control port

The first two reside inside the FDC IC while the Control port is in the external hardware. The addresses of these three ports are as follows.

|  |  |  |  |
| --- | --- | --- | --- |
| **Port Address [hex]** | **Port Name** | **Location** | **Port type** |
| 3F5 | Data port |  | Bidirectional I/O |
| 3F4 | Main status register | FDC IC | Input |
| 3F2 | Digital control port | External hardware | Output |

**Data port**

This port is used by the software for three different purposes:

* While issuing a command to the FDC IC, command and command parameter bytes are issued to the FDC IC through this port. The FDC IC stores the different parameters and the command in its internal registers.
* After a command is executed, the FDC IC stores a set of status parameters in the internal registers. These are read by the CPU through this port. The different status bytes are presented by the FDC IC in a specific sequence.
* In the programmed and interrupt mode of data transfer, the data port is used for transferring data between the FDC IC and the CPU IN or OUT instruction.

**Main status register (MSR)**

This port is used by the software to read the overall status information regarding the FDC IC and the FDD's. Before initiating a floppy disk operation the software reads this port to confirm the readiness condition of the FDC and the disk drives to verify the status of the previously initiated command. The different bits of this register represent:

|  |  |
| --- | --- |
| **Bit** | **Representation** |
| 0 | FDD 0: Busy in seek mode |
| 1 | FDD 1: Busy in seek mode |
| 2 | FDD 2: Busy in seek mode |
| 3 | FDD 3: Busy in seek mode |
| 4 | FDC Busy; Read/Write command in progress |
| 5 | Non-DMA mode |
| 6 | DIO; Indicates the direction of data transfer between the FDC IC and the CPU |
| 7 | MQR; Indicates data register is ready for data transfer |

|  |  |
| --- | --- |
| **Explanations** |  |
| MQR | 1 = data register ready, 0 = data register not ready |
| DIO | 1 = controller has data for CPU, 0 = controller expecting data from CPU |
| Non-DMA | 1 = Controller Not in DMA Mode, 0 = Controller in DMA Mode |
| FDC Busy | 1 = Busy, 0 = Not Busy |
| FDD 0,1,2,3 | 1 = Running, 0 = Not Running |

### Digital control port

This port is used by the software to control certain FDD and FDC IC functions. The bit assignments of this port are:

|  |  |
| --- | --- |
| **Bit** | **Representation** |
| 0 and 1 | Device number to be selected |
| 2 | RESET FDC IC (Low) |
| 3 | Enable FDC interrupt and DMA request signals |
| 4 to 7 | Turn ON the motor in disk drive 0, 1, 2 or 3 respectively |